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UNITED STATES PATENT APPLICATION

FOR

ELIMINATION OF THE FAST-ERASE PHENOMENA IN FLASH MEMORY

BY

TUUNG LUOH, LING-WUU YANG, DONALD HUANG, AND

KUANG-CHAO CHEN

FINNEGAN
HENDERSON
FARABOW
GARRETT &
DUNNER LLP

1300 I Street, NW
Washington, DC 20005
202.408.4000
Fax 202.408.4400
www.finnegan.com

DESCRIPTION OF THE INVENTION

Field of the Invention

[001] This invention relates to a method of forming a semiconductor device and, more particularly, to a method of forming a floating gate memory cell in a non-volatile memory device.

Background of the Invention

[002] A floating gate semiconductor memory device generally includes a plurality of memory cells, each comprising a MOS transistor with a floating gate to store charges. The MOS transistor of the memory cell also includes a control gate, a source region, a drain region, a substrate, and a channel defined as the region between the source region and the drain region. A first insulating layer is formed between the substrate and the floating gate, and a second insulating layer is formed between the floating gate and the control gate. The source and drain regions of the MOS transistor serve as bit lines of the memory cell, while the control gate of the MOS transistor serves as a word line of the memory cell. Each of the control gate, the source, the drain, and the substrate constitutes a terminal of the MOS transistor, and bias voltages may be applied to these terminals. Through different biasing schemes, a bit of information may be written into or erased from the memory cell.

[003] During programming of the memory cell, bias voltages are applied to the terminals of the MOS transistor of the memory cell so that charges in the channel region, such as electrons, gain enough energy to tunnel through the first insulating layer between the substrate and the floating gate. This is generally known as "hot-electron tunneling." For example, the control gate may be biased at a

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DUNNER LLP

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Washington, DC 20005
202.408.4000
Fax 202.408.4400
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voltage level that is positive with respect to the bias at the source terminal or the drain terminal. As the charges tunnel through the first insulating layer to the floating gate, they are trapped in the floating gate, and, as a result, the threshold voltage of the MOS transistor is changed. Therefore, the threshold voltage can be an indicator of whether the memory cell is in a "0" state or a "1" state.

[004] To erase the information bit from the memory cell, a different bias scheme is applied to the MOS transistor so that a mechanism called Fowler-Nordheim tunneling takes place, and charges stored in the floating gate may "tunnel" out from the floating gate. Fowler-Nordheim tunneling mechanism is well-known to one skilled in the art and will not be described herein. One conventional method of erasing the information bit from a memory cell is to apply a negative bias at the control gate of the MOS transistor and a positive bias at the source terminal, while leaving the drain terminal of the MOS transistor floating. The bias at the negative control gate, together with the bias at the source region, creates an electrical field between the floating gate and the source that forces the electrical charges stored in the floating gate to tunnel to the source region through the first insulating layer. As such, this method is known as "source tunneling."

[005] However, when these charges tunnel from the floating gate to the source region, there also exists a band-to-band tunneling, i.e., carriers tunneling between two energy bands, over the overlap region between the control gate and source region. This unintended and undesirable band-to-band tunneling becomes more substantial as devices are scaled down in size to adversely effect the operations of the memory device.

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[006] Another method of erasing a bit of information stored in the floating ate is to bias the substrate, the source, and the drain of the MOS transistor of the memory cell at a similar voltage level, while biasing the control gate of the memory cell at a voltage level that is negative with respect to the substrate bias. Thus, electron tunneling takes place over the entire channel region of the MOS transistor, and band-to-band tunneling is decreased. This method of erasing is known as "channel erasing," and is generally considered faster than source erasing.

[007] However, because the erasing operation is performed over a plurality of memory cells at the same time, and these memory cells may not be uniform in size or threshold voltages, the channel erasing method may result in some of the cells being "overly erased," i.e., the channel region being depleted, and consequently, current leakages between neighboring bit lines, to adversely effect the operations of the memory device.

SUMMARY OF THE INVENTION

[008] In accordance with the present invention, there is provided a method of forming a semiconductor device that includes providing a semiconductor substrate, forming a first insulating layer over the semiconductor substrate, forming a floating gate over the first insulating layer with a reaction gas, wherein the floating gate comprises a microcrystalline material having a grain size of about 50-300Å, forming a second insulating layer over the floating gate, and forming a control gate over the second insulating layer.

[009] Also in accordance with the present invention, there is provided a method of forming a semiconductor device that includes providing a silicon

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Washington, DC 20005
202.408.4000
Fax 202.408.4400
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substrate, selective doping of the silicon substrate to form a plurality of bit lines in the silicon substrate, forming a first insulating layer over the silicon substrate, forming a floating gate over the first insulating layer, wherein the floating gate comprises an amorphous material, thermally treating the memory cell to transform the amorphous material into a microcrystalline material, forming a second insulating layer over the floating gate, and forming a control gate over the second insulating layer.

[010] Still in accordance with the present invention, there is provided a method of forming a semiconductor memory device that includes providing a semiconductor silicon substrate, forming a plurality of bit lines in the silicon substrate, depositing a first insulating layer over the silicon substrate including the plurality of bit lines, forming a floating gate over the first insulating layer, wherein the floating gate comprises one of amorphous material or a microcrystalline material having a grain size of 50-300Å, forming a second insulating layer over the floating gate, forming a plurality of word lines over the second insulating layer, and forming a layer of nitride over the plurality of word lines.

[011] Additional features and advantages of the invention will be set forth in part in the description which follows, and in part will be obvious from the description, or may be learned by practice of the invention. The features and advantages of the invention will be realized and attained by means of the elements and combinations particularly pointed out in the appended claims.

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GARRETT &
DUNNER LLP

1300 I Street, NW
Washington, DC 20005
202.408.4000
Fax 202.408.4400
www.finnegan.com

[012] It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

[013] The accompanying drawing, which is incorporated in and constitutes a part of this specification, illustrates embodiments of the invention and, together with the description, serves to explain the objects, advantages, and principles of the invention.

[014] In the drawing,

[015] Fig. 1 shows a semiconductor device manufactured using the method according to an embodiment of the present invention.

DESCRIPTION OF THE EMBODIMENTS

[016] According to the present invention, there is provided a method of forming a memory device, particularly a floating gate memory device. Such a memory device may include a plurality of memory cells, each for storing at least one bit of information. Each memory cell comprises a MOS transistor with a floating gate, a control gate, a source region, a drain region, a channel region defined between the source and drain regions, and a substrate. The control gate serves as part of one word line of the memory cell, and the source and drain regions serve as parts of two bit lines of the memory cell.

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202.408.4000
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[017] The method of forming a memory device 100 according to an embodiment of the present invention includes providing a semiconductor substrate 102. Semiconductor substrate 102 may be comprised of silicon or any other semiconductor material used in semiconductor technology. The conductivity type of the semiconductor substrate can be either p-type or n-type. Through conventional masking steps, selective doping of the semiconductor substrate is performed to form a plurality of bit lines, or source region 104 and drain region 106 of the MOS transistors (not numbered). The selective doping process may be performed with any conventional method, such as ion implantation, and diffusion. The dopant used in this step may be either n-type or p-type, depending on the conductivity type of the substrate. Source region 104 and drain region 106 of each MOS transistor also define a channel region 108 therebetween.

[018] After the formation of the bit lines, a first insulating layer 110 is formed over the surface of semiconductor substrate 102 having bit lines 104 and 106 formed thereon. First insulating layer 110 may be comprised of oxide, nitride, or any other dielectric material or combination thereof commonly used in the art. A floating gate 112 is then formed over first insulating layer 110 and is electrically insulated from the substrate 102 by first insulating layer 110. In one aspect, floating gate 112 is comprised of amorphous silicon. In another aspect, floating gate 112 is comprised of microcrystalline polysilicon. In one aspect, the microcrystalline polysilicon has a grain size of about 50-300Å. In another aspect, the microcrystalline polysilicon has a grain size of about 200-600Å.

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202.408.4000
Fax 202.408.4400
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[019] Floating gate 112 may be formed with conventional chemical vapor deposition (CVD) method using a combination of gases that is comprised of a reaction gas and an optional second gas. In one aspect, the reaction gas is comprised of SiX, Si_2Y, or any appropriate combination thereof, wherein X is comprised of one or more of H_4, H_2Cl_2, HCl_3, D_4, D_2Cl_2, and D_3Cl, and Y is comprised of one or more of H6, H_4Cl_2, H_2Cl_4, D_6, D_4Cl_2, and D_2Cl_4. In another aspect, the optional second gas is comprised of at least one or more of D_2, H_2, and D_3.

[020] In one embodiment, the step of forming floating gate 112 comprises forming a layer of microcrystalline polysilicon over first insulating layer 110 with a grain size of about 50-300Å, followed by a thermal treatment to increase the grain size to about 200-600Å. In one aspect, the thermal treatment is performed in a conventional vertical furnace or rapid thermal process apparatus, with reaction gases including N_2, O_2, H_2, N_2O. In another aspect, the thermal treatment is performed at a temperature of about 800°C - 1000°C.

[021] In another aspect, the step of forming floating gate 112 comprises forming a layer of amorphous silicon over first insulating layer 110. A step of thermal treatment follows to transform the amorphous silicon into polysilicon with a grain size of about 200-500Å. In one aspect, the thermal treatment is performed in a conventional vertical furnace or rapid thermal process apparatus, with reaction gases including N_2, O_2, H_2, N_2O. In another aspect, the thermal treatment is performed at a temperature of about 800°C - 1000°C.

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[022] Compared to a conventionally formed polysilicon gate, the floating gate of the present invention exhibits a higher gate coupling ratio (GCR), an improved swing degradation, and a lower electron-trapping rate for the first and second insulating layers.

[023] Following the formation of floating gate 112, a second insulating layer 114 is formed over floating gate 112. Second insulating layer 114 may be comprised of oxide, nitride, or any other dielectric material commonly used in the art, or a combination thereof. A control gate 116 is then formed over second insulating layer 114. Control gate 116 may be comprised of polysilicon or any gate material commonly used in the art.

[024] In one aspect, a cap layer 118 is further formed over the surface of control gate 116. Cap layer 118 may be comprised of silicon nitride (SiN). In operation, nitride cap layer 118 over control gate 116 improves the performance of the memory device, e.g., the difference in the threshold voltage of the MOS transistor for different memory cell, i.e., "0" and "1", is increased, and the endurance of memory device 100 is improved.

[025] Conventional semiconductor manufacturing processes follow to complete the formation of the memory device and necessary circuits that accompany a memory device.

[026] Compared to a flash memory device fabricated using a conventional process, the flash memory provided by the present invention has a higher and more stable cell read current, and therefore has a better operation performance.

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[027] It is to be understood that, although the method of forming a floating gate in the present invention has been described in conjunction with the fabrication of a memory device, it may as well be applied in other situations that would benefit from the microcrystalline structures so formed.

[028] It will be apparent to those skilled in the art that various modifications and variations can be made in the disclosed process without departing from the scope or spirit of the invention. Other embodiments of the invention will be apparent to those skilled in the art from consideration of the specification and practice of the invention disclosed herein. It is intended that the specification and examples be considered as exemplary only, with a true scope and spirit of the invention being indicated by the following claims.

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